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Technical Review of D Type Flip Flops

Introduction

This paper is a review of the Data (or delay) Flip Flop (DFF) technology. It is called the delay flip flop, because the output follows the input on a positive clock edge. DFFs on the market can include anywhere from a single DFF to as much as eight flip flops on a single IC chip. These DFF will make up the heart off the finite state machine that will hold the car's current gear, and output a logic signal to a microcontroller corresponding to the gear/state the user is in. For this project I will only need three DFF to make eight distinguished state, or gears, so I will review only single, and dual DFFs.

Commercial Applications & Products

The commercial applications of this flip flop mainly involve bounce elimination switch, data storage, data transfer, latch, registers, counters, frequency division, and memory [1]. For our case, we will be using it for data storage, the data being which state/gear the vehicle is currently in. Jameco Electronics sells a dual DFF for $0.59 each, Mouser Electronics sells a single type DFF for $0.37 each, and Digi-Key Electronics sells a single type DFF for $0.43 each. Jameco's dual DFF is the cheapest cost per FF, and operates at the standard Vcc of 5 volts. Mouser sells single low power consumption DFF that can operate between 1.65 – 5.5 volts Vcc [2]. Digi-Key's single DFF operates at the same Vcc range, however, Digi-Key's is packaged in a smaller package, and can support ultra-high clock speeds [3]. The Mouser DFF can be clocked up to 150 MHz higher than Mouser and Jameco, which clock at 20-25 MHz.

Underlying Technology

The underlying technology behind the flip flop is a pulse steering circuit, and a NAND gate latch. Both the steering circuit and latch are comprised of two NAND gates. The input D, goes into one of the steering gates, and also goes through an inverting NAND gate, and then into the second steering gate. A clock signal feeds into both the steering gates. The outputs of the steering circuit gates each go into a separate gate in the latch circuit. The other two inputs of the latch come from the latch outputs. For

example, the output of gate A goes into the input of gate B, and vice versa. With this specific topology, the D flip-flop output Q tries to follow the input D but cannot make the required transitions unless it is enabled by the rising clock edge [4]. Most often, the set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. Note: The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation [5].

Building Blocks for Implementation

The building blocks for implementing the DFF in this state machine first starts out with a Moore state diagram, because the output only depends on which state/gear the user is in. After the building the state diagram, a Karnaugh map will define the characteristic equations governing the state machine. The K-map will also help minimize the extra components needed to distinguish between the different inputs for the states. [6]. The last component needed is a clock source, which will come from the microcontroller that governs the power flow from the battery to the motor depending on specific state outputs.

References

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